REMARKS

This Supplemental Amendment is filed in order to facilitate processing in the above-identified application. In particular, claims 13 and 19 have been amended for stylistic reasons. It is respectfully submitted that the amendment to the claims is unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claims. It is respectfully requested that the Examiner approves the correction.

Thus it now appears that the application is now in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Ellen Marcie Emas, Registration No. 32,131

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620
Date: August 14, 2002

Marked-up Claims 13 and 19

13. (Amended) A semiconductor device comprising:

an active area with at least one MOS transistor to be formed therein; and

an insulation film for defining said active area,

said active area having a recess in plan configuration,

said recess being defined by first, second and third edges,

said first and second edges being parallel to each other, with said insulation film positioned therebetween,

said third edge being connected to a first end of said first edge and first end of said second edge, said third edge extending in a direction perpendicular to a direction in which said first and second edges extend,

said active area having a fourth edge connected to a second end opposite from said first end of said first edge, said fourth edge being parallel to said third edge, said fourth edge extending in a direction opposite from said second edge,

said at least one MOS transistor including

a first MOS transistor having a first gate electrode, and

a second MOS transistor having a second gate electrode,

said first gate electrode extending in a direction perpendicular to the direction in which said fourth edge extends, said first gate electrode having a first end extending beyond said fourth edge over said insulation film,

said second gate electrode extending in a direction perpendicular to the direction in which said third edge extends, said second gate electrode having a first end extending beyond said third edge over said insulation film,

Marked-up Claims 13 and 19

said first gate electrode beyond said fourth edge being defined by having a first length from said fourth edge to said first end thereof, said second gate electrode beyond said third edge being defined by having a second length from said third edge to said first end thereof, [said second] the length of said second gate electrode being greater than [said first] the length of said first gate electrode.

19. (Amended) A method of manufacturing a semiconductor device including an active area with at least one MOS transistor to be formed therein, and an insulation film for defining said active area, based on layout design comprising the steps of:

(a) configuring said active area to have a recess in plan configuration; and

(b) configuring a first MOS transistor having a first gate electrode and a second MOS transistor having a second gate electrode on said active area,

said step (a) including the steps of

configuring said recess to be defined by first, second and third edges, said first and second edges being parallel to each other, with said insulation film positioned therebetween,

said third edge being connected to a first end of said first edge and a first end of said second edge, said third edge extending in a direction perpendicular to a direction in which said first and second edges extend, and

configuring a fourth edge connected to a second end opposite from said first end of said first edge, said fourth edge being parallel to said third edge, said fourth edge extending in a direction opposite from said second edge,

Marked-up Claims 13 and 19

said step (b) including the steps of

configuring said first gate electrode to extend in a direction perpendicular to the direction in which said fourth edge extends and to have a first and end extending beyond said fourth edge over said insulation film, and

configuring said second gate electrode to extend in a direction perpendicular to the direction in which said third edge extends and to have a first end extending beyond said third edge over said insulation film,

said first gate electrode beyond said fourth edge being defined by having a first length from said fourth edge to said first end thereof, said second gate electrode beyond said third edge being defined by having a second length from said third edge to said first end thereof, [said second] the length of said second gate electrode being greater than [said first] the length of said first gate electrode.